

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference 00000PCT7497	FOR FURTHER ACTION	
See item 4 below		
International application No. PCT/JP2004/016797	International filing date (<i>day/month/year</i>) 05 November 2004 (05.11.2004)	Priority date (<i>day/month/year</i>) 14 November 2003 (14.11.2003)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant SEMICONDUCTOR ENERGY LABORATORY CO., LTD.		

<p>1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 bis.1(a).</p> <p>2. This REPORT consists of a total of 6 sheets, including this cover sheet.</p> <p>In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.</p>																									
<p>3. This report contains indications relating to the following items:</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%; text-align: center; padding: 5px;"><input checked="" type="checkbox"/></td> <td style="width: 15%; text-align: center; padding: 5px;">Box No. I</td> <td style="width: 70%; padding: 5px;">Basis of the report</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. II</td> <td style="padding: 5px;">Priority</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. III</td> <td style="padding: 5px;">Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. IV</td> <td style="padding: 5px;">Lack of unity of invention</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input checked="" type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. V</td> <td style="padding: 5px;">Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. VI</td> <td style="padding: 5px;">Certain documents cited</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. VII</td> <td style="padding: 5px;">Certain defects in the international application</td> </tr> <tr> <td style="text-align: center; padding: 5px;"><input type="checkbox"/></td> <td style="text-align: center; padding: 5px;">Box No. VIII</td> <td style="padding: 5px;">Certain observations on the international application</td> </tr> </table>		<input checked="" type="checkbox"/>	Box No. I	Basis of the report	<input type="checkbox"/>	Box No. II	Priority	<input type="checkbox"/>	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability	<input type="checkbox"/>	Box No. IV	Lack of unity of invention	<input checked="" type="checkbox"/>	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement	<input type="checkbox"/>	Box No. VI	Certain documents cited	<input type="checkbox"/>	Box No. VII	Certain defects in the international application	<input type="checkbox"/>	Box No. VIII	Certain observations on the international application
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<input type="checkbox"/>	Box No. VIII	Certain observations on the international application																							
<p>4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44bis .2).</p>																									

<p>The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland</p> <p>Facsimile No. +41 22 740 14 35</p>	<p>Date of issuance of this report 15 May 2006 (15.05.2006)</p> <p>Authorized officer Masashi Honda</p> <p>Telephone No. +41 22 338 70 10</p>
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PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

REC'D 03 FEB 2005

PCT WIPO PCT

To:
**SEMICONDUCTOR ENERGY
LABORATORY CO., LTD.
398, HASE, Atsugi-shi, Kanagawa
2430036 Japan**

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year)

01.2.2005

Applicant's or agent's file reference
00000PCT7497

FOR FURTHER ACTION

See paragraph 2 below

International application No.
PCT/JP2004/016797

International filing date (day/month/year)

05.11.2004

Priority date (day/month/year)

14.11.2003

International Patent Classification (IPC) or both national classification and IPC
Int.Cl' **H01L29/786**

Applicant

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

1. This opinion contains indications relating to the following items:

- Box No. I Basis of the opinion
- Box No. II Priority
- Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- Box No. IV Lack of unity of invention
- Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- Box No. VI Certain documents cited
- Box No. VII Certain defects in the international application
- Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Date of completion of this opinion

12.01.2005

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

4L 9361

KAZUNARI TANADA

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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/016797

Box No. I Basis of the opinion

1. With regard to the language, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any nucleotide and/or amino acid sequence disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

a. type of material

a sequence listing
 table(s) related to the sequence listing

b. format of material

in written format
 in computer readable form

c. time of filing/furnishing

contained in the international application as filed.
 filed together with the international application in computer readable form.
 furnished subsequently to this Authority for the purposes of search.

3. In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/ 016797

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims <u>1-24</u>	YES
	Claims	NO
Inventive step (IS)	Claims <u>1-24</u>	YES
	Claims	NO
Industrial applicability (IA)	Claims <u>1-24</u>	YES
	Claims	NO

2. Citations and explanations

D1 : JP 2003-234355 A(SEMICONDUCTOR ENERGY LABORATORY CO., LTD.),
2003.08.22, paragraphs [0056]-[0086], Fig.1-6 (Family : none)
D2 : JP 02-000025 A(CANON KABUSHIKI KAISHA), 1990.01.05,
lines 7-11, column 4, page 4, Fig.1 (Family : none)
D3 : GB 2211992 A(SEIKOSHA CO. , LTD.), 1989.07.12, Fig 5 & JP 01-179368 A
D4 : JP 2003-318192 A(SEIKO EPSON CORPORATION), 2003.11.07,
paragraphs [0051],[0073],[0074] (Family : none)
D5 : JP 06-275645 A(SHARP KABUSHIKI KAISHA), 1994.09.30,
paragraph [0013] (Family : none)

Claims 1-6

The subject matters of claims 1-6 do not appear to involve an inventive step in view of D1 and D2. D1 discloses a semiconductor element comprising a gate electrode layer; a semiconductor film; a pair of n-type impurity regions formed over the semiconductor film; an insulating film that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer formed over the pair of n-type impurity regions; wherein a thickness of a portion of the semiconductor film over which the insulating film is formed is thinner than that of the other semiconductor film. D2 discloses a layer comprising titanium formed over a substrate. The thin film transistor in D1 and D2 are concerned with mutually related technical fields. Therefore, the skilled person in the art would easily conceive the idea of applying the technical feature employed in D2 to the invention disclosed in D1.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: V. 2

Claims 7, 10, 12

The subject matters of claims 7, 10, 12 do not appear to involve an inventive step in view of D3 and D4. D3 discloses a method for manufacturing a semiconductor element comprising: forming a gate electrode layer; forming a gate insulating film; forming a semiconductor film containing an impurity element having a conductivity type over the semiconductor film; forming a source electrode and a drain electrode over the semiconductor film containing the impurity element having the conductivity type; forming an insulating film over a portion of the semiconductor film; and forming an island-like semiconductor film by removing the semiconductor film using the source electrode, the drain electrode, and the insulating film as masks. D4 discloses a method for forming a gate electrode, source electrode and drain electrode by discharging a composite containing a conductive material. The thin film transistors in D3 and D4 are concerned with mutually related technical fields. Therefore, the skilled person in the art would easily conceive the idea of applying the technical feature employed in D4 to the invention disclosed in D3.

Claims 8, 11

The subject matters of claims 8, 11 do not appear to involve an inventive step in view of D2 to D4. D2 discloses a layer comprising titanium formed over a substrate. The thin film transistors in D2 to D4 are concerned with mutually related technical fields. Therefore, the skilled person in the art would easily conceive the idea of applying the technical features employed in D2 and D4 to the invention disclosed in D3.

Claim 9

The subject matters of claim 9 do not appear to involve an inventive step in view of D2 to D5. D5 discloses a insulating film comprising at least one selected from the group consisting of organic material. The thin film transistors in D2 to D5 are concerned with mutually related technical fields. Therefore, the skilled person in the art would easily conceive the idea of applying the technical features employed in D2, D4 and D5 to the invention disclosed in D3.

Claims 13-18

The subject matters of claims 13-18 do not appear to involve an inventive step in view of D1 and D2. D1 discloses a semiconductor element comprising a gate electrode layer; a semiconductor film; a pair of n-type impurity regions formed over the semiconductor film; an insulating film that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer formed over the pair of n-type impurity regions; wherein a thickness of a portion of the semiconductor film over which the insulating film is formed is thinner than that of the other semiconductor film. D2 discloses a layer comprising titanium formed over a substrate. The thin film transistor in D1 and D2 are concerned with mutually related technical fields concerning a liquid crystal display device. Therefore, the skilled person in the art would easily conceive the idea of applying the technical feature employed in D2 to the invention disclosed in D1.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: V.2

Claims 19, 22, 24

The subject matters of claims 19, 22, 24 do not appear to involve an inventive step in view of D3 and D4. D3 discloses a method for manufacturing a semiconductor element comprising: forming a gate electrode layer; forming a gate insulating film; forming a semiconductor film containing an impurity element having a conductivity type over the semiconductor film; forming a source electrode and a drain electrode over the semiconductor film containing the impurity element having the conductivity type; forming an insulating film over a portion of the semiconductor film; and forming an island-like semiconductor film by removing the semiconductor film using the source electrode, the drain electrode, and the insulating film as masks. D4 discloses a method for forming a gate electrode, source electrode and drain electrode by discharging a composite containing a conductive material. The thin film transistors in D3 and D4 are concerned with mutually related technical fields concerning a liquid crystal display device. Therefore, the skilled person in the art would easily conceive the idea of applying the technical feature employed in D4 to the invention disclosed in D3.

Claims 20, 23

The subject matters of claims 20 and 23 do not appear to involve an inventive step in view of D2 to D4. D2 discloses a layer comprising titanium formed over a substrate. The thin film transistors in D2 to D4 are concerned with mutually related technical fields concerning a liquid crystal display device. Therefore, the skilled person in the art would easily conceive the idea of applying the technical feature employed in D2 and D4 to the invention disclosed in D3.

Claim 21

The subject matter of claim 21 does not appear to involve an inventive step in view of D2 to D5. D5 discloses a insulating film comprising at least one selected from the group consisting of organic material. The thin film transistors in D2 to D5 are concerned with mutually related technical fields. Therefore, the skilled person in the art would easily conceive the idea of applying the technical features employed in D2, D4 and D5 to the invention disclosed in D3.